

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 6,897,517
APPLICATION NO. : 10/603426
ISSUE DATE : May 24, 2005
INVENTOR(S) : Van Houdt et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On page 1, at section (73) Assignees, after "Infineon" please insert --Technologies--.

On page 1, at section (73) Assignees, please delete "Munich" and insert therefore --Neubiberg--.

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DOCKET NO. IMEC279.001AUS



US006897517B2

(12) **United States Patent**
Van Houdt et al.

(10) **Patent No.:** **US 6,897,517 B2**
 (45) **Date of Patent:** **May 24, 2005**

(54) **MULTIBIT NON-VOLATILE MEMORY AND METHOD**

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(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** 10/603,426

(22) **Filed:** Jun. 24, 2003

(65) **Prior Publication Data**

US 2004/0057264 A1 Mar. 25, 2004

Related U.S. Application Data

(60) **Provisional application No.** 60/391,565, filed on Jun. 24, 2002.

(51) **Int. Cl.⁷** H01L 29/788

(52) **U.S. Cl.** 257/315; 257/239; 257/261; 257/316; 257/317; 257/320; 257/321; 438/201; 438/211; 438/216; 438/241; 438/257; 438/260

(58) **Field of Search** 257/239, 261, 257/298, 315-326; 438/201, 211, 216, 241, 257-258, 260-266, 591, 593

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,794,565 A	12/1988	Wu et al.	
5,278,439 A	1/1994	Ma et al.	
5,280,446 A	1/1994	Ma et al.	
5,284,784 A	2/1994	Manley	
5,338,952 A	8/1994	Yamauchi	
5,394,360 A	2/1995	Fukumoto	
5,538,811 A	7/1996	Kanbara et al.	
5,587,332 A	* 12/1996	Chang et al.	438/258
6,044,015 A	3/2000	Van Houdt et al.	
6,366,500 B1	4/2002	Ogura et al.	

6,580,120 B2 6/2003 Haspeslagh
 2002/0005545 A1 1/2002 Widdershoven et al.

FOREIGN PATENT DOCUMENTS

EP 1 096 572 A1 5/2001

OTHER PUBLICATIONS

US 5,841,697, 11/1998, Van Houdt et al. (withdrawn)
 Esquivel, et al., "High density contactless, self aligned EPROM cell array technology", IEDM Tech. Dig., pp. 592-595, (1986).
 Hayashi, et al., "Twin MONOS cell with dual control gates", IEEE, presented at the 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 122-123, (2000).
 Microlithography, Science and Technology, Sheats, et al., Eds., Marcel Dekker, Inc., New York, New York, pp. 515-565 and 615-644, (1998).
 Miyawaki, et al., "A new erasing and row decoding scheme for low supply voltage operation 16-Mb/64-Mb flash memories", IEEE Journal of Solid-State Circuits, vol. 27, No. 4, pp. 583-588, (Apr. 1992).

(Continued)

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(57)

ABSTRACT

A memory is described having a semiconductor substrate of a first conductivity type, a first and a second junction region of a second conductivity type, whereby said first and said second junction region are part of respectively a first and a second bitline. A select gate is provided which is part of a wordline running perpendicular to said first and said second bitline.

Read, write and erase functions for each cell make use of only two polysilicon layers which simplifies manufacture and each memory cell has at least two locations for storing a charge representing at least one bit.

13 Claims, 21 Drawing Sheets

